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1. (Currently Amended) A read only memory (ROM) cell connected to a true bitline and a complement bitline, said ROM cell comprising:

a first transistor having a first drain; and

a second transistor having a second drain,

wherein said first drain is connected to said true bitline and said second drain is connected to said complement bitline,

wherein said first transistor further comprises a first source, and said second transistor further comprises a second source, [and]

wherein only one of said first source and said second source is connected to ground, and

wherein a connection of one of said first source and said second source to ground programs said ROM cell.

2. (Cancelled).

3. (Previously Amended) A read only memory (ROM) cell connected to a true bitline and a complement bitline, said ROM cell comprising:

a first transistor having a first drain; and

a second transistor having a second drain,

wherein said first drain is connected to said true bitline and said second drain is connected to said complement bitline,

wherein said first transistor further comprises a first source, and said second transistor further comprises a second source,

wherein a connection of one of said first source and said second source to a ground programs said ROM cell, and

wherein only one of said first source and said second source is connected to said ground and the other of said first source and said second source is insulated from electrical connections.

4. (Original) The ROM cell in claim 2, wherein said connection comprises an electrical connection formed during manufacturing of said first transistor and said second transistor.

5. (Original) The ROM cell in claim 1, wherein said first transistor further comprises a first gate connected to a wordline and said second transistor further comprises a second gate connected to said wordline.

6. (Original) The ROM cell in claim 1, wherein said second transistor comprises a complement transistor to said first transistor.

7. (Original) The ROM cell in claim 1, wherein said ROM cell shares said first drain and said second drain with corresponding drains of an adjacent ROM cell in said array.

8. (Currently Amended) A read only memory (ROM) cell array connected to a true bitline and a complement bitline, each ROM cell in said ROM cell array comprising:

a first transistor having a first drain; and

a second transistor having a second drain,

wherein said first drain is connected to said true bitline and said second drain is connected to said complement bitline,

wherein said first transistor further comprises a first source, and said second transistor further comprises a second source, [and]

wherein only one of said first source and said second source is connected to ground, and

wherein a connection of one of said first source and said second source to ground programs said ROM cell.

9. (Cancelled).

10. (Previously Amended) A read only memory (ROM) cell connected to a true bitline and a complement bitline, said ROM cell comprising:

a first transistor having a first drain; and

a second transistor having a second drain,

wherein said first drain is connected to said true bitline and said second drain is connected to said complement bitline,

wherein said first transistor further comprises a first source, and said second transistor further comprises a second source,

wherein a connection of one of said first source and said second source to a ground programs said ROM cell, and

wherein only one of said first source and said second source is connected to said ground and the other of said first source and said second source is insulated from electrical connections.

11. (Original) The ROM cell array in claim 9, wherein said connection comprises an electrical connection formed during manufacturing of said first transistor and said second transistor.

12. (Original) The ROM cell array in claim 8, wherein said first transistor further comprises a first gate connected to a wordline and said second transistor further comprises a second gate connected to said wordline.

13. (Original) The ROM cell array in claim 8, wherein said second transistor comprises a complement transistor to said first transistor.

14. (Original) The ROM cell array in claim 8, wherein said ROM cell shares said first drain and said second drain with corresponding drains of an adjacent ROM cell in said array.

15. (Previously Amended) A method of forming a read only memory (ROM) cell, said method comprising:

forming a first drain of a first transistor such that said first drain is connected to a true bitline;

forming a second drain of a second transistor such that said second drain is connected to a complement bitline; and

forming a first source of said first transistor and a second source of said second transistor such that only one of said first source and said second source is connected to ground,

wherein a connection of only one of said first source and said second source to said ground programs said ROM cell.

16. (Cancelled).

17. (Currently Amended) A method of forming a read only memory (ROM) cell, said method comprising:

forming a first drain of a first transistor such that said first drain is connected to a true bitline;

forming a second drain of a second transistor such that said second drain is connected to a complement bitline; and

forming a first source of said first transistor and a second source of said second transistor such that one of said first source and said second source is connected to ground,

wherein a connection of only one of said first source and said second source to said ground programs said ROM cell, and

wherein said forming of said first source and said second source only connects one of said first source and said second source to said ground and insulates the other of said first source and said second source from electrical connections.

18. (Original) The method in claim 15, further comprising:

forming a first gate of said first transistor connected to a wordline; and

forming a second gate of said second transistor connected to said wordline.

19. (Original) The method in claim 15, wherein said second transistor comprises a complement transistor to said first transistor.

20. (Original) The method in claim 15, wherein said forming of said first drain and said second drain is performed such that said ROM cell shares said first drain and said second drain with corresponding drains of an adjacent ROM cell.

21-26. (Cancelled).